

Applicant(s): S.R. Cebenko et al.
Case: 1-1-3-1-1
Serial No.: TBA
Filing Date: February 14, 2002
Group: TBA

LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

14971 U.S. PTO
10/082050
02/14/02

U.S. PATENT DOCUMENTS

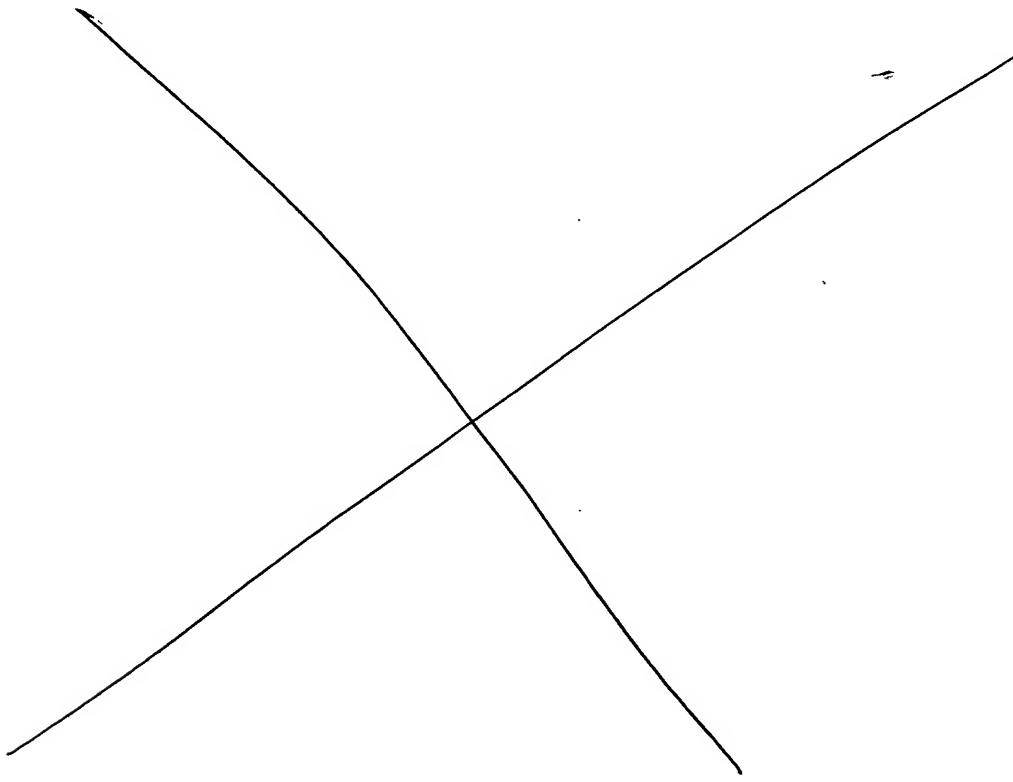
EXAMINER	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE
INITIAL					IF APPROPRIATE
<i>dlr</i>	09/400,029	9/21/99	J.A. Schadt, "Integrated Circuit With Standard Cell Logic and Spare Gates."		

FOREIGN PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION
INITIAL					YES NO

OTHER DOCUMENTS

EXAMINER	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
INITIAL		



Examiner

W. Rao

Date Considered

03/30/04

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.